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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,894	09/07/2005	James Knapp	ONS00407	3486

7590 10/11/2006

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/524,894	KNAPP ET AL	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *17-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/524894 Attorney's Docket #: ONS00407
Filing Date: 9/7/2005;

Applicant: Knapp et al.

Examiner: Alexander Williams

This application is a 371 of PCT/US02/28883 filed 9/10/2002.

Applicant's election of Group I (claims 1 to 16), filed 7/18/06, has been acknowledged.

This application contains claims 17 to 19 drawn to an invention non-elected without traverse.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 4-7 and 9-14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Yakida (Japan Patent # 10-289921).

1. Yakida (figures 1 to 4) specifically figure 4 show a semiconductor device, comprising: a semiconductor die **1**; and an inductor including a first bonding wire **16** attached to a top surface of the semiconductor die and extended laterally a distance greater than a height of the bonding wire to define an insulating core.

2. The semiconductor device of claim 1, Yakida show wherein the first bonding wire has first and second ends respectively attached to first and second bonding pads **5-8** on the top surface.

4. The semiconductor device of claim 1, Yakida show wherein the first bonding wire is formed with a coil that surrounds the insulating core.

5. The semiconductor device of claim 4, Yakida show wherein first and second ends of the first bonding wire are attached to first and second bonding pads, respectively, on the top surface and the coil is formed with a plurality of turns.

6. The semiconductor device of claim 5, Yakida show wherein the first bonding wire has an inductance greater than about five nanohenries.

7. The semiconductor device of claim 1, Yakida further comprises a semiconductor package for housing the semiconductor die and the inductor.

8. The semiconductor device of claim 7, Yakida show wherein the first bonding wire is attached to a first bonding pad of the semiconductor die, further comprising a second bonding wire attached between a second bonding pad of the semiconductor die and a lead of the semiconductor package.

9. The semiconductor device of claim 7, Yakida show wherein the semiconductor package includes an encapsulant for providing the insulating core and for maintaining a position of the coil.

10. The semiconductor device of claim 1, Yakida show wherein the first bonding wire provides an inductance and the semiconductor die includes an oscillator operating at a frequency determined by the inductance.

11. The semiconductor device of claim 10, Yakida show wherein the frequency is greater than two gigahertz.

12. The semiconductor device of claim 1, Yakida show wherein the bonding wire has a substantially circular cross-section.

13. Yakida (figures 1 to 4) specifically figure 4 show a semiconductor device, comprising: a semiconductor die **1**; and a bonding wire **16** electrically coupled to the semiconductor die and having a first portion formed in a coil around a dielectric core and a second portion extending vertically from a surface of the semiconductor device.

14. The semiconductor device of claim 13, Yakida show wherein the bonding wire is attached to first and second bonding points defining a line, and an axis of the dielectric core is substantially parallel to the line.

16. The semiconductor device of claim 13, Yakida further comprises a semiconductor package for housing the semiconductor

die and the bonding wire and having a lead that provides the surface for attaching the bonding wire.

Claims 1, 4-8, 12, 13 and 16 are rejected under 35 U.S.C. § 102(b) as being anticipated by (Japan Patent # 6-140451).

1. (Japan Patent # 6-140451) figures 1 and 2 show a semiconductor device, comprising: a semiconductor die **1**; and an inductor including a first bonding wire **12** attached to a top surface of the semiconductor die and extended laterally a distance greater than a height of the bonding wire to define an insulating core.

4. The semiconductor device of claim 1, (Japan Patent # 6-140451) show wherein the first bonding wire is formed with a coil that surrounds the insulating core.

5. The semiconductor device of claim 4, (Japan Patent # 6-140451) show wherein first and second ends of the first bonding wire are attached to first and second bonding pads, respectively, on the top surface and the coil is formed with a plurality of turns.

6. The semiconductor device of claim 5, (Japan Patent # 6-140451) show wherein the first bonding wire has an inductance greater than about five nanohenries.

7. The semiconductor device of claim 1, (Japan Patent # 6-140451) further comprises a semiconductor package for housing the semiconductor die and the inductor.

8. The semiconductor device of claim 7, (Japan Patent # 6-140451) show wherein the first bonding wire is attached to a first bonding pad of the semiconductor die, further comprising a second bonding wire attached between a second bonding pad of the semiconductor
die and a lead of the semiconductor package.

12. The semiconductor device of claim 1, (Japan Patent # 6-140451) show wherein the bonding wire has a substantially circular cross-section.

13. (Japan Patent # 6-140451) figures 1 and 2 show a semiconductor device, comprising: a semiconductor die **1**; and a bonding wire **12** electrically coupled to the semiconductor die and having a first portion formed in a coil around a dielectric core and a second portion extending vertically from a surface of the semiconductor device.

16. The semiconductor device of claim 13, (Japan Patent # 6-140451) further comprises a semiconductor package for housing the semiconductor die and the bonding wire and having a lead that provides the surface for attaching the bonding wire.

Claims 1, 2, 4 and 7 are rejected under 35 U.S.C. § 102(b) as being anticipated by Van Schuylenbergh et al. (European Patent 1 202 296 A1)..

1. Van Schuylenbergh et al. (figures 1 to 16B) specifically figure show a semiconductor device, comprising: a semiconductor die **210**; and an inductor **200** including a first bonding wire **260** attached to a top surface of the semiconductor die and extended laterally a

distance greater than a height of the bonding wire to define an insulating core.

2. The semiconductor device of claim 1, Van Schuylenbergh et al. show wherein the first bonding wire has first and second ends respectively attached to first and second bonding pads on the top surface.

4. The semiconductor device of claim 1, Van Schuylenbergh et al. show wherein the first bonding wire is formed with a coil that surrounds the insulating core.

7. The semiconductor device of claim 1, Van Schuylenbergh et al. further comprises a semiconductor package for housing the semiconductor die and the inductor.

Claims 1, 2 and 6-14, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Lee et al. (WO # 00/10179).

1. Lee et al. (figures 1 to 26) specifically figure 1 show a semiconductor device, comprising: a semiconductor die **9**; and an inductor including a first bonding wire **1** attached to a top surface of the semiconductor die and extended laterally a distance greater than a height of the bonding wire to define an insulating core.

2. The semiconductor device of claim 1, Lee et al. show wherein the first bonding wire has first and second ends respectively attached to first and second bonding pads on the top surface.

6. The semiconductor device of claim 5, Lee et al. show wherein the first bonding wire has an inductance greater than about five nanohenries.

7. The semiconductor device of claim 1, Lee et al. further comprises a semiconductor package for housing the semiconductor die and the inductor.

8. The semiconductor device of claim 7, Lee et al. show wherein the first bonding wire is attached to a first bonding pad of the semiconductor die, further comprising a second bonding wire attached between a second bonding pad of the semiconductor die and a lead of the semiconductor package.

9. The semiconductor device of claim 7, Lee et al. show wherein the semiconductor package includes an encapsulant for providing the insulating core and for maintaining a position of the coil.

10. The semiconductor device of claim 1, Lee et al. show wherein the first bonding wire provides an inductance and the semiconductor die includes an oscillator operating at a frequency determined by the inductance.

11. The semiconductor device of claim 10, Lee et al. show wherein the frequency is greater than two gigahertz.

12. The semiconductor device of claim 1, Lee et al. show wherein the bonding wire has a substantially circular cross-section.

13. Lee et al. (figures 1 to 26) specifically figure 1 a semiconductor device, comprising: a semiconductor die **9**; and a bonding wire **1** electrically coupled to the semiconductor die and having a first portion formed in a coil around a dielectric core and a second portion extending vertically from a surface of the semiconductor device.

14. The semiconductor device of claim 13, Lee et al. show wherein the bonding wire is attached to first and second bonding points defining a line, and an axis of the dielectric core is substantially parallel to the line.

Claims 3 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yahida (Japan Patent # 10-289921) in view of (Japan Patent # 06-140451).

Yahida show the features of the claimed invention as detailed above, but fail to explicitly show the first bonding wire is extended from the first and second bonding pads to vertically overlie an edge of the top surface and wherein the axis is substantially parallel to an edge of the semiconductor die.

(Japan Patent # 06-140451) is cited for showing a semiconductor IC device. Specifically, (Japan Patent # 06-140451) discloses (figures 1 and 2) the first bonding wire is extended from the first and second bonding pads to vertically overlie an edge of the top surface and wherein the axis is substantially parallel to an edge of the semiconductor die for the purpose of using piece of bonding wire with inductance portion which enables power supply noise reduction and prevents voltage reflection.

Therefore, it would have been obvious to one of ordinary skill in the art to use (Japan Patent # 06-140451) bonding wires to modify Yahida's bonding wires for the purpose of using piece of bonding wire with inductance portion which enables power supply noise reduction and prevents voltage reflection.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/528,532,531,535,728,784,786,690-693,696,698,666,676,685,723,724,725	8/7/06
Other Documentation: foreign patents and literature in 257/528,532,531,535,728,784,786,690-693,696,698,666,676,685,723,724,725	8/7/06
Electronic data base(s): U.S. Patents EAST	8/7/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
8/7/06